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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,071	11/19/2003	Darren L. Anand	BUR920030168US1	1070

23389 7590 01/11/2008

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EXAMINER
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ART UNIT	PAPER NUMBER
2117	

MAIL DATE	DELIVERY MODE
01/11/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/707,071	ANAND ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/14/2007 has been entered.

This is a Non-FINAL Office Action in response to the Amendment filed 10/15/2007.

Claims 1-25 are presently under examination and still pending in the Application.

Rejection of Claims 23-25 are under 35 U.S.C. 112, second paragraph, because of the expression “can be”, has been withdrawn in view of the amendment to the claims.

Response to Arguments

Applicant's arguments filed 10/15/2007, with respect to Claims 1-25, have been fully considered but they are not persuasive.

In reference to independent Claims 1, 7, 13 and 17, as currently amended, Applicant argues that the claimed invention allows for capturing all diagnostic fails data and transferring the data to the tester in a single test pass using an efficient interface.

In response to Applicant's argument, the Examiner notes that such a limitation is nowhere to be found either in the claims or in the specification. Instead, the claims, as

currently amended, merely recite a BIST for generating a fail map data including all diagnostic fails for capture by a diagnostic register device under control of a high speed multiplied clock.

According to Nadeau-Dostie, the transfer register 180 captures diagnostic summary data from the failure data selector 178, which operates under control of the Clock signal and a small finite state machine (FSM) 182. The transfer register has a serial input and a serial output and a clock input which receives the Clock signal. FSM 42 includes a counter 184 which counts the number of bits which have been loaded/unloaded into/from the transfer register. Clearly, the Transfer Register 180, as disclosed by Nadeau-Dostie, captures the diagnostic summary data associated with all the failures in the embedded memory 152 under test.

Furthermore, with respect to Fig. 3, Nadeau-Dostie describes when the test of a column or row has been completed, column or row failure summary is generated (step 47), loaded into a transfer register, and scheduled to be transferred off-chip (step 48) under the control of the ExtClock of the tester. The failure summary is transferred serially. However, the summary may also be transferred in parallel. After completing a test phase, when the last column (or row) has been tested (step 50), a phase failure summary may be generated and transferred off-chip (step 54).

In general, it is noted that the features upon which applicant relies in some of his arguments are not recited in the rejected claims. For example, Applicant argues that the method steps 36-52, Fig. 3 of Nadeau-Dostie are unnecessary in the method of the present invention because a failure summary is not needed. In Paragraph [0018],

Nadeau-Dostie describes, a failure summary is generated for each column during memory test phases that use a column access mode and for each row during memory test phases that use a row access mode. Memory test phases are executed at a first clock rate. Failure summaries are transferred from a memory test controller to an external tester at a second, lower, clock rate. Clearly, the failure summary corresponds to Applicant's claimed feature of "fail map data" including all diagnostic fails for capture by a diagnostic register device (transfer register 180) under control of a high speed multiplied clock.

Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 IFed. Cir. 1993).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 7, 8, 13, 17-19 and 23-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Nadeau-Dostie et al. (US 20050047229) US Application 10/690594, filed: October 23, 2003.

Regarding independent Claims 1, 7, 13, 17, Nadeau-Dostie discloses a method and a circuit for collecting memory failure information 164 on-chip and unloading the information in real time while performing at-speed test of an embedded memory 152 using a memory test controller 150, Fig. 7, comprising:

Using a high speed (system clock) for testing each memory location of the column or row of a memory under test (152) according to a memory test algorithm under the control of the system clock, and transferring the failure summary via a circuit serial output under the control of an (ExtClock) tester clock concurrently with testing of the next column or row in sequence, see Summary of the Invention. The system clock is multiple and synchronous with the ExtClock, as shown in Fig. 9,which is a detailed timing diagram, showing the (system clock) used to perform the memory test, and the ExtClock, which generates the synchronization pulses (SyncPulse) to synchronize the transfer of the failure summary to the tester.

During read operations, the memory data output is compared (step 30) against an expected value. If the data is different, a failure has been detected and is classified (step 34) according to predetermined failure types, thus pausing the testing at the end of a column or row test.

Using the ExtClock of the tester to read bit fail data from the failure summary block 164 out to the tester. When the test of a column or row has been completed,

column or row failure summary is generated (step 47), loaded into a transfer register, and scheduled to be transferred off-chip (step 48) under the control of the ExtClock. The failure summary is transferred serially. However, the summary may also be transferred in parallel. After completing a test phase, when the last column (or row) has been tested (step 50), a phase failure summary may be generated and possibly encoded (step 52) and transferred off-chip (step 54).

Resuming the BIST testing with the high speed (system clock) by beginning the test phase (step 20), and by next performing read and write operations (step 28) according to a memory test algorithm under control of the system clock.

Regarding Claim 2, 8, Nadeau-Dostie discloses a method and a circuit for collecting memory failure information 164 on-chip and unloading the information in real time while performing at-speed test of an embedded memory 152, such as a Static Random Access Memory (SRAM) and Dynamic Random Access Memory (DRAM) bitmaps of interest and potential failure causes, as shown in Fig. 2.

Regarding Claims 18, 19, Nadeau-Dostie discloses Failure data selector 178 loads summary data to be output from the circuit into a transfer register 180 and may also encode data according to a predetermined encoding scheme. Alternatively, data could be encoded prior to delivery to selector 178. The data loaded into the transfer register depends on the specific failure summary combination, which was designed for the circuit, the access mode and phase of a test. The transfer register operates under control of the Clock signal and a small finite state machine (FSM) 182. The transfer register has a serial input and a serial output and a clock input which receives the Clock

signal. FSM 42 includes a counter 184, which counts the number of bits, which have been loaded/unloaded into/from the transfer register.

Regarding Claims 23-25, new fail map data are captured in the failure summary generator block 164, using a high speed (system clock), Figs. 8 and 9.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-6, 9-12, 14-16 and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nadeau-Dostie et al. (US 20050047229) in view of Hirabayashi (US Patent No. 6,978,402).

Regarding Claims 3, 4, 6, 9, 10, 12, 14, 16, 20, 22, Nadeau-Dostie does not explicitly disclose, "an on-chip clock multiplier to multiply the external clock to generate a high speed multiplied clock and a multiplexer to pass either the tester clock or the high speed multiplied clock".

However, in analogous art, Hirabayashi (US Patent No. 6,978,402) discloses a clock generator 11, Figs. 3-6, which receives an external clock signal CK and includes an oscillator 111, which generates a high-frequency clock signal, and a multiplexer 113,

which selects, as an internal clock signal CK_int, the external clock signal CK_ext or the high-frequency clock signal. In a normal mode, the multiplexer 113 selects the external clock signal CK_ext as the internal clock signal CK_int. In a high-speed test mode, the multiplexer 113 selects the high-frequency clock signal generated by the oscillator 111 as the internal clock signal CK_int.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to employ the clock generator as taught by Hirabayashi in the embedded memory test controller of Nadeau-Dostie for the purpose of carrying out high-speed testing of embedded memories using built-in self test (BIST) circuit, thus avoiding the use of expensive High-speed testers.

Regarding Claims 5, 11, 15, 21, Nadeau-Dostie discloses a failure summary generator 164, which receives various inputs from comparators block 162 at a system clock rate, but transfers failure summary to a tester at a tester clock rate, which is usually significantly lower than the system clock rate, Figs. 7 and 8. After completing a test phase, when the last column (or row) has been tested (step 50), a phase failure summary may be generated and possibly encoded (step 52) and transferred off-chip (step 54), Fig. 3.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques H. Louis-Jacques can be reached on (571) 272-4150. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Date: 4 January 2008
Office Action: Final Rejection

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1/4/08

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